REMARKS/ARGUMENTS

This is in response to an Office action dated 10/13/2005.

Status
Claims 1-20 are pending
Claims 1-16 are rejected
Claims 17-20 are withdrawn from consideration

Rejection(s) under 35 USC §102

Claims 1-3, 5, 7, 11 and 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hu et al. (US 6,660,627 B2). The Examiner states that,

Re **claim 1**, Hu discloses a method of forming an interconnect structure comprising the steps of:

depositing a dielectric layer **(38)**;
forming a hard mask over the dielectric material **(40)**;
etching trenches **(44)** in the dielectric material;
depositing a liner material **(46)** over the hard mask **(40)** and within the trenches **(50)**; and
overfilling the trenches **(44)** with a conductive material **(48)**;

characterized by:

performing a first chemical mechanical polishing process to remove conductive material **(48)** which is atop the liner **(46)** thereby exposing the liner **(46)**; (Note: Fig. 2D)
removing that portion of the liner **(46)** which is atop the hard mask **(40)**; (Note: Fig. 2E)
removing a first portion of the hard mask **(42)** using a wet etch process, thereby leaving in place a second portion of the hard mask (40); and (Note: Fig. 2F)
performing a touch-up polishing process to remove conductive material and liner material protruding from the trenches. (Note: Col. 3, Line 41- Col. 4, Line 60)

Re **claim 2**, pertaining to claim 1 above, Hu discloses the dielectric layer comprising a low-k material. (Note: Col 3, Lines 4-5)

Re claim 3, pertaining to claim 1 above, Hu discloses the dielectric layer comprising an ultra low-k material. (Note: Col 3, Lines 4-5)

Re claim 5, pertaining to claim I above, Hu discloses the conductive material comprising copper. (Note: Col 3, Lines 37-40)

Re claim 7, pertaining to claim 1 above, Hu discloses the portion of the liner, which is atop the hard mask is removed by a second chemical mechanical polishing process. (Note: Col 4, Lines 19-35)

Re **claim 11**, pertaining to claim 1 above, Hu discloses the second portion of the hardmask comprising a silicon carbide (SiC) material. -.

Re **claim 13**, pertaining to claim 1 above, Hu discloses the touch-up polishing process using an abrasive-free or low-abrasive polish to obtain a very high selectivity between the conductive material and the second portion of the hard mask. (Note: Col 4, Lines 36-59)

Re **claim 14**, Hu discloses the method of forming an interconnect structure comprising the steps of:

depositing a dielectric material (38);
forming a hard mask over the dielectric material **(40)**;

etching trenches in the dielectric material **(44)**; and
overfilling the trenches with a conductive material **(44)**;
characterized by:
performing a first chemical mechanical polishing step;
then, performing a wet etch step; and
then, performing a second chemical mechanical polishing step. (Note: Cot 3, Lines 4-5)

Re **claim 15**, pertaining to claim 14 above, Hu discloses at least a portion of the hard masks. is substantially intact. (Note: Fig. 2F)

Re **claim 16**, pertaining to claim 14 above, Morrow discloses the portion of the hard mask, which is left substantially intact, comprises a silicon carbide SiC material (Note: Fig. 2F)

Rejection(s) under 35 U.S.C. §103

Claims 4, 8-10 and 12 are rejected under 35 U S C 103(a) as being unpatentable over Hu et at (US 6,660,627 B2), as applied in Paragraph 5 above, and in view of Morrow (US 6,872,666 B2).

The Examiner states that,

Re **claim 4**, as applied to claim 1 in Paragraph 5 above, Hu discloses all the claimed limitations including a silicon carbide or oxide hard mask

However, Hu does not specifically disclose, wherein, the hard mask comprises a layer of silicon carbide material atop the dielectric layer, and a layer of oxide atop the layer of silicon carbide.

Morrow discloses the method of making a damascene interconnect using a dual hard mask comprising a: a layer of silicon carbide material atop the dielectric layer **(103)**, and a layer of oxide **(108)** atop the layer of silicon carbide **(109)** (Note Col 3 Lines 1-26)

Both Hu and Morrow teachings are directed to fabricating a interconnect forming a dual mask. Therefore, the teachings of Hu and Morrow are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide the Hu reference with a dual hard mask of a layer of silicon carbide material atop the dielectric layer, and a layer of oxide atop the layer of silicon carbide as taught by Morrow in order to form an interconnect because the dual hard mask enables different portions of dielectric layer. (Note: Col 3, Line 4- Line7)

Re **claim 8**, as applied to claim 1 in Paragraph 5 above, Hu discloses all the claimed limitations including a silicon carbide or oxide hard mask.

However, Hu does not specifically disclose, wherein, the hard mask comprises: a layer of silicon carbide material atop the dielectric layer, and a layer of oxide atop the layer of silicon carbide.

Morrow discloses the method of making a damascene interconnect using a dual hard mask comprising a: a layer of silicon carbide material atop the dielectric layer **(103)**, and a layer of oxide **(108)** atop the layer of silicon carbide **(109)**. (Note: Col 3, Lines 1-26)

Both Hu and Morrow teachings are directed to fabricating a interconnect forming a dual mask. Therefore, the teachings of Hu and Morrow are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide the Hu reference with a dual hard mask of a layer of silicon carbide material atop the dielectric layer, and a layer of oxide atop the layer of silicon carbide as taught by Morrow in order to form an interconnect because the

dual hard mask enables different portions of dielectric layer. (Note: Col 3, Line 4- Line7)

Re **claim 9**, as applied to claim 8 in the paragraph above, Hu discloses ensuring that the oxide portion of the hard mask is thick enough such that the topographical variations after the first chemical mechanical polishing process and liner removal are entirely within the oxide portion of the hard mask. (Note: Fig. 2)

Re **claim 10**, as applied to claim 8 in the paragraph above, Hu discloses an oxide with a thickness smaller than 1000 Angstrom.

Re claim 12, as applied to claim 1 in Paragraph 5 above, Hu discloses all the claimed limitations including a silicon carbide or oxide hard mask.

However, Hu does not specifically disclose, wherein, the hard mask comprises: a layer of silicon carbide material atop the dielectric layer, and a layer of oxide atop the layer of silicon carbide.

Morrow discloses the method of making a damascene interconnect using a dual hard mask comprising a: a layer of silicon carbide material atop the dielectric layer **(103)**, and a layer of oxide **(108)** atop the layer of silicon carbide **(109)**. (Note: Col 3, Lines 1-26)

Both Hu and Morrow teachings are directed to fabricating a interconnect forming a dual mask. Therefore, the teachings of Hu and Morrow are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide the Hu reference with a dual hard mask of a layer of silicon carbide material atop the dielectric layer, and a layer of oxide atop the layer of silicon carbide as taught by Morrow in order to form an interconnect because the dual hard mask enables different portions of dielectric layer. (Note Col 3 Line 4- Line7)

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et at. (US 6,660,627 B2), as applied above, and in view of Allen et at. "Substrate Smoothing Using Gas Cluster Ion Beam Processing." The Examiner states:

Re claim 6, as applied to claim 1 in Paragraph 5 above, Hu discloses all the claimed limitations.

However, Hu does not specifically disclose, wherein the portion of the liner which is atop the hard mask is removed by a reactive ion etch (RIE) or a Gas Cluster Ion Beam (GCIB) process.

Allen discloses the method of using a gas cluster ion beam for surface smoothing. (Note Abstract)

Both Hu and Allen teachings are directed to the smoothing of a substrate with chemical metal polishing and gas cluster ion beam, respectively. Therefore the teachings of Hu and Allen are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide the Hu reference with the gas cluster ion beam processing as taught by Allen in order to obtain thin films with smooth, atomic layer control of the surface finish with the occurrence of sub-surface damage. (Note: Col 1, Lines 1-3).

The Invention, Generally

The invention is generally directed to maintaining uniform CMP hard mask thickness. A chemical mechanical polishing (CMP) step is used to remove excess conductive material (e.g., Cu) overlying a low-k or ultralow-k interlevel dielectric layer (ILD) layer having trenches filled with

conductive material, for a damascene interconnect structure. A reactive ion etch (RIE) or a Gas Cluster Ion Beam (GCIB) process is used to remove a portion of a liner which is atop a hard mask. A wet etch step is used to remove an oxide portion of the hard mask overlying the ILD, followed by a final touch-up Cu CMP (CMP) step which chops the protruding Cu patterns off and lands on the SiCOH hard mask. In this manner, processes used to remove excess conductive material substantially do not affect the portion of the hard mask overlying the interlevel dielectric layer.

The References, Generally

Hu et al. (US 6,660,627 B2) discloses method for planarization of wafers with high selectivities. A method for planarization of a semiconductor wafer with a high selectivity is described. The semiconductor wafer has a hard mask, a stop layer disposed on the hard mask, and a barrier layer disposed on the stop layer. The method includes performing a chemical mechanical polishing (CMP) process on the barrier layer so as to expose the stop layer, and removing the stop layer. The polishing selectivity of the barrier layer relative to the stop layer is greater than 50. Since the material of stop layer is different from the material of barrier layer, the high selectivity is easily achieved. Thus, the surface of semiconductor wafer can be highly planarized.

Morrow (US 6,872,666 B2) discloses method for making a dual damascene interconnect using a dual hard mask. Initially, a structure is formed that includes first and second hard masking layers that cover a dielectric layer. A first part of the second hard masking layer and a first part of the first hard masking layer are etched to form an etched region within the hard mask that exposes a first portion of the dielectric layer. That etched region is filled with a sacrificial material. After etching through a second part of the second hard masking layer, the remainder of the sacrificial material is removed prior to subsequent processing.

Allen et at. "Substrate Smoothing Using Gas Cluster Ion Beam Processing." discloses substrate smoothing using gas cluster ion beam processing. In order to smooth a wide variety of surface material types to within an angstrom of roughness without subsurface damage, a beam energy equivalent to the individual bond energy of the surface atoms would be required. This would ideally preserve the integrity of the underlying material matrix and eliminate both high and low frequency surface aberrations. A low energy ion beam of a few hundred eV would be difficult to produce with significant intensity, however, due to the space charge effect encountered from the increase in density of the ions produced ("beam blow-up"). The use of a gas cluster ion beam (GCIB) process, however, has proven to provide an effective atomic smoothing on numerous material surface compositions without causing subsurface damage. Allen provides a description of the recently developed GCIB surface smoothing and modification apparatus, a discussion of the mechanism for surface smoothing, and provides a focus on thin film Si, SiC, and semiconductor-on-insulator (SOI) material results.

Comments Traversing the Rejection(s)

As described in the specification, a damascene interconnect structure comprises:

trenches formed in an ILD defined by openings in a hard mask (HM) overlying the ILD,
a liner which covers the top surface of the HM, and surfaces of the trenches,
damascene material (for example, copper) overfilling the trenches.

The general idea is to remove excess copper.

The HM comprises a silicon carbide material with a layer of oxide on top.

The silicon carbide material functions as a polish stop. The silicon carbide material is in the range of 50 – 5000A, such as 100A to 1000A.

The oxide HM is thick enough to ensure that topographical variations after Cu CMP are entirely within the oxide HM. The oxide HM is in the range of 50 – 5000A, such as 100A to 1000A.

Cu CMP is performed, and proceeds only as far as the liner. See FIG. 2.

Next, liner (over the HM) is removed. See FIG. 3. The copper is protruding.

Next, oxide HM is removed. See FIG. 4. The copper is protruding. The silicon carbide HM is in place.

Finally, a CMP "touch up" process is performed to remove the protruding copper (and residual liner on the sides of the copper). See FIG. 5. The silicon carbide HM is in place.

In Hu (6,660,627), see Figs, 2A-2F, there is
a dielectric layer 38, and
a hard mask 40 is formed on the dielectric layer 38, and a stop layer 42 is formed on the hard mask 40.
Hu's hard mask 40 is made from typical photoresist material, such as SiO_2, SiN, SiON, SiC, SiCO, or SiOCN and has a thickness that is smaller than 1000A.

In the present invention, the analogous silicon carbide material is in the range of 50 – 5000A, such as 100A to 1000A. A thickness of 1000-5000A is outside of the range of Hu.

Hu's stop layer 42 is composed of organic polymer material, and a thickness of the stop layer 42 is smaller than 1000 A, preferably 200 to 400 A.

In the present invention, the analogous second HM layer is oxide and has a thickness in the range of 50 – 5000A, such as 100A to 1000A.. A thickness of 1000-5000A is outside of the range of Hu.
Via openings 44 are formed. See Fig. 2B. (compare trenches of the present invention).

A barrier layer 46 is deposited. See Fig. 2C. (compare liner of the present invention).

Thereafter, as shown in Fig. 2D, a first chemical mechanical polishing (CMP) process is performed for exposing the barrier layer 46 and the via plug 50. Compare present invention, FIG. 2.

Next as shown in Fig. 2E, a second CMP process is performed on the barrier layer 46 so as to expose the stop layer 42. The mechanism of the second CMP process generates chemical

reactions on the surface of the barrier layer 46 from the material of the barrier layer 46 and appropriate chemicals, which are slurry with a suitable pH value and a related oxidizer. Meanwhile, an appropriate solvent is utilized for generating considerable affinity between the surface of the barrier layer 46 and abrasive particles of the slurry. Then, a mechanical strength of 0.5 to 10 psi provided by a polishing pad is exerted so as to execute the second CMP process. According to the preferred embodiment of the present invention, a polishing apparatus is the Mirra Mesa polishing machine available from the Applied Materials or the polishing machine of type 776 available from the SpeedFam-IPEC Company. The polishing pad is the K-XY GROOVE polishing pad from the Rodel IC series made from polyurethane (PU) foam. The slurry is the base slurry Rodel-1501 having silica as the abrasive particles.

This step (removing the liner) of the present invention is different than Hu,

> In a next step, the portion of the liner which is over the hard mask is removed. (The portion of the liner which is within the trench is not affected in this, or in any other step.) This is done using either a reactive ion etch (RIE) or a Gas Cluster Ion Beam (GCIB) process. These processes are highly selective to the material of the liner (tantalum, etc.) over the Oxide HM. And, the copper remains substantially intact during this process. The resulting interim (partially completed) interconnect structure is shown in **FIG. 3** wherein it can be observed that the copper from within the trenches protrudes slightly (e.g., substantially equal to the original thickness of the liner), above the level of the Oxide HM. (The "copper line" is slighly higher than the Oxide HM.)

Next, when the second CMP process of the barrier layer 46 has been completed, then the stop layer 42 is removed. The stop layer 42 may be removed by a third CMP process. The stop layer 42 may also be removed by a dry etching process or a wet etching process.

Here, the present invention differs from Hu.

In the present invention, the Oxide HM is removed, using a suitable process such as hydrogen fluoride (HF) wet etch. The resulting interim (partially completed) interconnect structure is shown in **FIG. 4**. Again, it can be observed that the copper from within the trenches protrudes slightly. AND, finally, a CMP "touch up" process is performed to remove the conductive material (e.g., copper) and liner material protruding from the trenches. See **FIG. 5**.

The problem is that if the hard mask is "just" polished (as in Hu), there can be a problem because chemistry causes a polish rate for copper that is much faster than that for the dielectric. Therefore the copper "wears down" faster than the dielectric. When the copper was "thick" it wasn't such a problem. But now the copper in the circuit pattern is much thinner and the copper wears down too much during the time it takes to wear down the dielectric. This leads to increased resistance and slower chip performance.

The solution to the problem is in the last touch up process.

1) The chemistry for polishing the hard mask can be the same abrasive slurry as in the first (top) layer.
2) The abrasive is non-abrasive or low abrasive
3) the is a low cleaning force of .1-2 psi preferably .2-.5 psi

4) there is no polishing of the hard mask

The claims are amended to clarify the differences, as discussed hereinabove.

step/structure	HU 6660627	Present Invention
two layers of hard mask	40 carbide 42 polymer	carbide oxide
thickness of first HM layer	<1000A	50-5000A **1000-5000A is outside HU**
thickness of 2nd HM layer	<1000A	50-5000A **1000-5000A is outside HU**
liner	yes	yes
overfill	yes	yes
Cu CMP to liner	Fig 2D, using CMP-1	FIG 2, using CMP
remove liner to top HM	Fig 2E, using CMP-2 copper is also planarized	FIG 3, using **RIE or GCIB** **copper remains/protrudes**
remove stop layer	Fig 2F, using CMP-3, or dry/wet etch	FIGs 4 and 5. **two steps.** using wet etch followed by "touch up" CMP

Claim 1, as amended, now sets forth the method of forming a hard mask comprising a layer of silicon carbide (SiC) material overlying a dielecteric layer and etching trenches in the dielectric material; depositing a liner material over the hard mask and within the trenches. The method includes performing a first chemical mechanical polishing process to remove conductive material which is atop the liner, thereby exposing the liner. The claim also sets forth removing that portion of the liner which is atop the hard mask.....leaving conductive material protruding, removing the layer of oxide using a wet etch process, leaving the layer of silicon carbide and performing a touch-up polishing process to remove conductive material protruding from the trenches. None of the references taken alone or in combination teach or suggest performing a touch-up polishing process to remove conductive material protruding from the trenches. Therefore claim 1, should be deemed allowable.

Claims 2-5, 9-11, and claim 13 depend upon claim 1 and should also be deemed allowable.

Newly-presented independent claim 21 is similar to claim 1, with the added limitation of dielectric material from claims 2 and 3 and should therefore be deemed allowable.

Newly-presented claims 22-28 are dependent upon claim 21, are similar to the remaining ones of claims 4-11 and should therefore be deemed allowable.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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